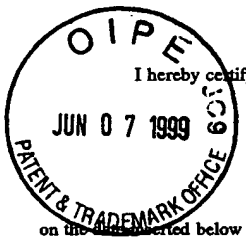
AF/GAU 3651

PATENT
Attorney Docket No.2972US



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June 7, 1999 — Date of Deposit

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No.:	08/715,869	Group Art Unit No.:	3651
Filing date:	September 19, 1996	Examiner:	T. Nguyen
For (title):	METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUITS		

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION – 37 C.F.R. § 192)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on April 5, 1999.

2. STATUS OF APPLICATION
This application is on behalf of
- ☒ other than a small entity
- ☐ small entity

verified statement:
- ☐ attached
- ☐ already filed

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 C.F.R. § 1.17(f) the fee for filing the Appeal Brief is:

☐ small entity status	$150
☒ other than a small entity	$300

4. EXTENSION OF TIME

☐ A petition for Extension of Time for a month extension of time for filing the Appeal Brief is enclosed.

5. FEE PAYMENT

- ☒ Check No. 11804 is enclosed in payment of the fee for filing the Appeal Brief plus any extension of time for which a petition has been filed.
- ☐ Please charge this fee to deposit account No. 20-1469 (a duplicate copy of this notice is enclosed--see below).

Any additional appeal fees which are not otherwise submitted herewith or which are insufficient should be charged to deposit account no. 20-1469. A duplicate copy of this notice is enclosed. Please address all communications in connection with this appeal to the address indicated below.

06/11/1999 SSALEEKU 00000078 08715869
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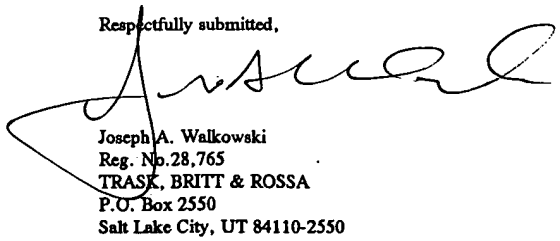
Respectfully submitted,



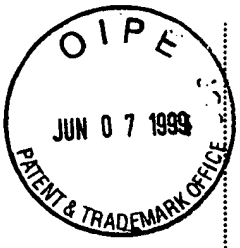
Joseph A. Walkowski
Reg. No.28,765
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, UT 84110-2550
(801) 532-1922

Date: June 7, 1999
Enclosures: As identified above

PATENT

#17
6-15-99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES



In re Application of:

Steve W. Heppler

Serial No.: 08/715,869

Filed: September 19, 1996

For: METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUITS

Examiner: Nguyen, T

Group Art Unit: 3651

Attorney Docket No.: 2972US (92-0476RE)

NOTICE OF EXPRESS MAILING

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BRIEF ON APPEAL

Assistant Commissioner for Patents
Washington, D.C. 20231
Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is in furtherance of the Notice of Appeal, filed in this case on April 5, 1999, and is submitted in triplicate in the format of 37 C.F.R. § 1.192(c), and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., assignee of the pending application as set forth in the Notice of Merger of Micron Semiconductor, Inc. with Micron Technology, Inc., recorded with the United States Patent and Trademark Office on September 19, 1996, at Reel 8323, Frame 0019.

(2) RELATED APPEALS AND INTERFERENCES

Neither the appellants, the appellants' representative, nor the assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF THE CLAIMS

Claims 1 through 32 are pending in the application.

Claims 1 through 6 have been allowed.

Claims 7 through 32 stand rejected.

Claims 7 through 32 are being appealed.

(4) STATUS OF AMENDMENTS

A Response to the Official Action dated July 9, 1998, was filed on October 5, 1998. The Response was submitted to overcome the Official Action's objection to FIG. 1 of the drawings, and the Official Action's rejection of claims 5 and 6 raised under 35 U.S.C. § 112, second paragraph, and claims 7 through 32 raised under 35 U.S.C. § 102(b) for anticipation. The

Response included amendments to the paragraph appearing in column 1, lines 14 through 34, of the specification, and FIG. 1. No claims were amended in the Response. The proposed drawing correction was approved by the Office in the Final Office Action, dated January 12, 1999. Applicant believes that the amendment to the specification was entered.

A Final Office Action, dated January 12, 1999, was received by Applicant, rejecting claims 5 and 6 under 35 U.S.C. § 112, second paragraph, and claims 7 through 32 under 35 U.S.C. § 102(b). Applicant filed a response to the Final Office Action dated January 12, 1999. Applicant submitted a proposed amendment to claim 5. The Advisory Action received from the Office, dated March 23, 1999, indicates that upon filing an Appeal the proposed amendment will be entered. Applicant believes that this amendment has now been entered, and claims 1 through 6 are allowed and claims 7 through 32 continue to stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tateno (U.S. Patent 4,733,459).

Applicant has now appealed from the March 23, 1999, Final Office Action. The Notice of Appeal was filed on April 5, 1999.

(5) SUMMARY OF THE INVENTION

The present invention relates to an integrated circuit testing apparatus capable of testing individual integrated circuits and separating defective integrated circuits from working integrated circuits. (Specification at column 2, lines 15-18). The present invention also relates to a method of testing individual integrated circuits using the integrated testing apparatus.

A preferred embodiment of the integrated circuit testing apparatus of the present invention comprises a loading ramp or track (Drawing FIG. 2, element 16), a testing station (Drawing FIG.

2, element 18), and a separating station (Drawing FIG. 2, element 34). The testing station of the preferred embodiment of the integrated circuit testing apparatus further comprises a part guide (Drawing FIG. 2, element 24), an extractor bar (Drawing FIG. 2, element 26), an insertion bar (Drawing FIG. 2, element 28), a testing socket (Drawing FIG. 2, element 30), a stop pin (Drawing FIG. 2, element 22) positioned so as to define a device under test station (Drawing FIG. 2, element 20) and a holding station (Drawing FIG. 2, element 31) within the testing station, and a pin (Drawing FIG. 2, element 32) positioned to hold or allow an integrated circuit to pass from the testing station to the separating station. (Specification, column 2, lines 51 to 69). The testing station is movable between a first position and a second position, whereby the testing station in the first position receives an integrated circuit into the device under test station and the testing station tests an integrated circuit in the second position. (Specification, column 2, lines 59 to 61). The separating station comprises two tracks (Drawing FIG. 2, elements 36 and 38 respectively) for receiving integrated circuits.

A preferred method of testing an integrated circuit and separating non-defective integrated circuits from those that are defective using the integrated circuit testing apparatus of the present invention includes: receiving an integrated circuit to be tested from the loading ramp or track (Drawing FIG. 2, element 16) into the device under test station (Drawing FIG. 2, element 20) of the testing station (Drawing FIG. 2, element 18) in a first position with the stop pin (Drawing FIG. 2, element 22) positioned so as to maintain the integrated circuit in the device under test station; moving the testing station to a second position whereby the integrated circuit is inserted into a testing socket (Drawing FIG. 2, element 30) for testing (Specification, column 2, lines 59 to 61); returning the testing station to the first position and positioning the stop pin (Drawing

FIG. 2, element 22) so as to allow the integrated circuit to pass into the holding station (Drawing FIG. 2, element 31) (Specification, column 2, lines 63 to 66); positioning the pin (Drawing FIG. 2, element 32) so as to allow the integrated circuit to pass into the separating station (Drawing FIG. 2, element 34); the pin being positioned in such a manner that non-defective integrated circuits are allowed to pass onto the upper track (Drawing FIG. 2, element 36) (Specification, column 2, lines 66 to 68) while the testing station is in a first position and in such a manner that defective integrated circuits are allowed to pass onto the lower track (Drawing FIG. 2, element 38) while the testing station is in a second position. (Specification, column 3, lines 7 to 9).

(6) ISSUES

Whether claims 7 through 32 are anticipated under 35 U.S.C. § 102(b) by United States Patent 4,733,459 issued to Tateno.

(7) GROUPING OF CLAIMS

The grouping of the claims is as follows:

(a) Claim 7 is independently patentable. Claim 8 depends from claim 7 and stands or falls with claim 7.

(b) Claim 9 depends from claim 8, however, claim 9 is independently patentable and does not stand or fall with claim 8. Claim 9 stands or falls on its own.

(c) Claim 11 depends from, and stands or falls with, claim 10.

(d) Claim 12 is dependent upon claim 11, but does not stand or fall with claim 11. Claim 12 is independently patentable and stands or falls on its own.

(e) Claims 13 and 19 stand or fall together.

(f) Although claim 14 depends from claim 13, and claim 15 depends from claim 14, claims 14 and 15 do not stand or fall with claim 13. Likewise, claim 20 depends from claim 19, and claim 21 depends from claim 20, however, claims 20 and 21 do not stand or fall with claim 19. Claims 14, 15, 20, and 21 stand or fall together.

(g) Claim 16 stands or falls on its own.

(h) Claim 17 depends from claim 16 and claim 18 depends from claim 17. However, claims 17 and 18 do not stand or fall with claim 16. Instead, claims 17 and 18 stand or fall with each other.

(i) Claim 22 stands or falls on its own.

(j) Claim 23 depends from claim 22 but does not stand or fall with claim 22. Likewise, claim 24 depends from claim 23 and does not stand or fall with claim 22. Instead, claims 23 and 24 stand or fall together.

(k) Claim 25 stands or falls on its own.

(l) Claim 26 stands or falls on its own.

(m) Claim 27 is independently patentable. Claim 28 depends from claim 27 and stands or falls with claim 27.

(n) Claim 29 is independently patentable. Claim 30 depends from claim 29 and stands or falls with claim 29.

(o) Claim 31 stands or falls on its own.

(p) Claim 32 stands or falls on its own.

(8) ARGUMENT

35 U.S.C. § 102(b) Anticipation Rejection

Claims 7-32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tateno (U.S. Pat. 4,733,459).

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Brothers Inc. v. Union Oil Company of California, 2 USPQ2d 1051, 1053 (1987). For each and every element to be shown in a single piece of prior art "every element of the claimed invention must be literally present, arranged as in the claim." Richardson v. Suzuki Motor Co. Ltd., 9 USPQ2d 1913, 1920 (1989) (emphasis added). Contrary to the Examiner's assertions, the Tateno patent fails to expressly or inherently describe a "testing apparatus" or a "separating apparatus" as claimed with respect to the current invention, thus failing to provide a basis upon which a proper rejection for anticipation under 35 U.S.C. § 102(b) may stand. See, MPEP § 2131.

Tateno teaches "an electronic insertion apparatus...which can automatically insert ICs into a printed circuit board." *See, Tateno* at column 1, lines 65 to 67. Untested integrated circuits are gravitationally fed to a hand 44 which is in a first position. The hand 44 engages an integrated circuit at the first position and transfers the integrated circuit to a second position where the integrated circuit is inserted into a printed circuit board 15. *See, Tateno*, column 6, lines 47-54. The hand 44 then returns to the first position without the integrated circuit and repeats the process, filling a printed circuit board with untested integrated circuits. At no time does the hand 44, or any part of the Tateno apparatus, perform a test on the integrated circuits. The hand 44 of Tateno is incapable of testing integrated circuits and the reference fails to expressly or inherently

disclose, or even suggest, a "testing apparatus" which is in any way similar to that of the present invention. Such failure precludes an anticipation rejection under 35 U.S.C. § 102(b). *See* Verdegaal Brothers Inc., 2 USPQ2d at 1053.

The Examiner has indicated that the Tateno apparatus includes "a holding station 50, a first position and a second position." *See, Final Office Action* dated January 12, 1999, paragraph 3. As previously mentioned, the hand 44 alternates between a first position and a second position, yet the hand 44 fails to test the integrated circuit in the second position, as in the present invention. In addition, the "holding station 50" of the Tateno apparatus is an X-Y table portion 50, used to position a printed circuit board for receiving integrated circuits. This in no way anticipates the holding station (Drawing FIG. 2, element 31) of the testing station (Drawing FIG. 2, element 18) of the invention which is the issue of this appeal. Unlike the holding station of the present invention, the "holding station 50" of the Tateno patent fails to move between the first position and the second position of a testing apparatus. The failure of the Tateno patent to describe or anticipate a holding station as claimed and arranged in the present invention precludes an anticipation rejection under 35 U.S.C. § 102(b) because every element of the present invention is not disclosed by Tateno. *See* Verdegaal Brothers Inc., 2 USPQ2d at 1053.

Likewise, Tateno fails to describe a "separating apparatus" capable of separating defective integrated circuits from non-defective integrated circuits. First, the integrated circuits manipulated by the Tateno apparatus are never tested to determine whether or not they are defective, therefore, it is impossible to separate the integrated circuits by defective or non-defective condition. Second, the integrated circuits are attached to a printed circuit board and Tateno provides no method or apparatus by which defective circuits attached to the printed circuit

boards may detached and separated from the non-defective integrated circuits. Third, even if the elevator portion 60 of the Tateno patent is capable of separating defective integrated circuits from those that are non-defective, as proposed by the Examiner (Final Office Action, paragraph 3), the elevator portion 60 is devoid of any tracks upon which defective and non-defective integrated circuits could be separated. The failure of Tateno to disclose a "separating apparatus" having a "defective integrated circuit track...and a non-defective integrated circuit track," as in the present invention, precludes an anticipation rejection under 35 U.S.C. § 102(b) because each and every element of the present invention has not been disclosed. *See* Richardson, 9 USPQ2d at 1920.

Thus, the Section 102(b) rejection is without merit. However, Applicant will address the specific rejection as it applies to each group of claims.

(a) Claims 7 and 8

Claim 7 recites "a testing apparatus positioned to receive the untested integrated circuits from the receiving apparatus and test the integrated circuits to identify defective integrated circuits and non-defective integrated circuits." (emphasis added). Tateno fails to expressly or inherently disclose a testing apparatus capable of testing and identifying defective integrated circuits and non-defective integrated circuits.

Likewise, claim 7 recites "a separating apparatus...to separate defective integrated circuits from non-defective integrated circuits...including a defective integrated circuit track...and a non-defective integrated circuit track." Tateno fails to disclose a separating apparatus which is capable of separating defective integrated circuits from non-defective integrated circuits. In addition, Tateno's failure to disclose a defective integrated circuit track and a non-defective

integrated circuit track precludes a rejection under 35 U.S.C. § 102(b) for anticipation because each and every element of the claimed invention is not disclosed by the prior art. *See*, Verdegaal Brothers Inc. v. Union Oil Company of California, 2 USPQ2d 1051, 1053 (1987).

Claim 8 depends from claim 7 and is allowable therewith.

(b) Claim 9

Claim 9 is dependent from claim 8, but independently patentable. Claim 9 further recites "the holding station while in the first position...[allowing] non-defective integrated circuits to proceed to the non-defective integrated circuit track" and "while in the second position releasing defective integrated circuits to the defective integrated circuit track." Although the Examiner maintains that a "holding station 50" exists in the Tateno patent, the "holding station 50" of Tateno does not correspond to the holding station claimed in claim 9 of the present invention because the "holding station 50" of Tateno is not capable of movement with a testing apparatus between a first and a second position. In addition, the "holding station 50" of the Tateno patent inoperable to release defective integrated circuits or non-defective integrated circuits because the integrated circuits on the "holding station 50" of Tateno are untested. Likewise, Tateno's failure to disclose non-defective integrated circuit tracks and defective integrated circuits tracks precludes a rejection of claim 9 under 35 U.S.C. § 102(b) due to anticipation. Therefore, claim 9 is allowable.

(c) Claims 10 and 11

Claim 10 is independently patentable because it further recites "a loading apparatus for supplying the integrated circuit...to the integrated circuit testing apparatus," and "a receiving apparatus positioned to receive untested integrated circuits." Claim 10 also recites an integrated circuit testing apparatus and a separating apparatus "including a defective integrated circuit track...an a non-defective integrated circuit track." Neither the loading apparatus nor the receiving apparatus of claim 10 is disclosed or taught by Tateno, and, as previously stated, Tateno also fails to disclose each of the testing apparatus, the separating apparatus, the defective integrated circuit track, and the non-defective integrated circuit track. The failure of Tateno to teach the elements of claim 10 precludes an anticipation rejection of that claim under 35 U.S.C.. § 102(b).

Claim 11 depends from claim 10 and is allowable therewith.

(d) Claim 12

Claim 12 depends from claim 11 but is independently patentable. Claim 12 further recites "the holding station while in the first position...[allowing] non-defective integrated circuits to proceed to the non-defective integrated circuit track" and "while in the second position releasing defective integrated circuits to the defective integrated circuit track." Although the Examiner maintains that a "holding station 50" exists in the Tateno patent, the "holding station 50" of Tateno does not disclose a holding station as claimed in claim 12 of the present invention because the "holding station 50" of Tateno is inoperable to move with a testing apparatus between a first and a second position. In addition, the "holding station 50" of the Tateno patent cannot operate

to release defective integrated circuits or non-defective integrated circuits because the integrated circuits on the "holding station 50" of Tateno are untested. Likewise, Tateno's failure to disclose non-defective integrated circuit tracks and defective integrated circuits tracks precludes a rejection of claim 12 under 35 U.S.C. § 102(b) due to anticipation. Therefore, claim 12 is allowable.

(e) Claims 13 and 19

Claim 19 stands or falls with claim 13, which is independently patentable as a method of testing an integrated circuit.

Claim 13 recites a method of testing an integrated circuit in a testing apparatus comprising the steps of: "receiving the integrated circuit at the testing apparatus while...in the first position; moving the testing apparatus to the second position; testing the integrated circuit to identify defective and non-defective conditions of the integrated circuit; moving the testing apparatus to the first position to allow the tested integrated circuit to proceed to the holding station while receiving a second singulated integrated circuit...and separating the defective and non-defective integrated circuits." As previously indicated, Tateno fails to disclose any form of testing of integrated circuits and the Tateno apparatus is incapable of identifying "defective and non-defective" conditions of an integrated circuit. In addition, Tateno fails to disclose a method by which defective integrated circuits may be separated from non-defective integrated circuits.

(f) Claims 14-15 and 20-21

Claims 15, 20, and 21 stand or fall with claim 14 which is independently patentable. Claim

14 recites a method of testing an integrated circuit in a testing apparatus further including: "providing a testing apparatus with a non-defective and defective integrated circuit track; and...[preventing] defective integrated circuits from proceeding to the non-defective track, and allowing non-defective integrated circuits to proceed to the non-defective integrated circuit track." The absence of the foregoing elements from the Tateno disclosure or claims precludes a 35 U.S.C. § 102(b) rejection for anticipation because each and every element of the present invention is not disclosed as arranged in claim 14. Therefore, claim 14 is allowable. Likewise, claim 15, which depends from and stands or falls with claim 14, and claims 20 and 21, which stand or fall with claim 14, are allowable.

(g) Claim 16

Claim 16 is an independently patentable method of testing an integrated circuit. Claim 16 recites a method of testing an integrated circuit comprising the steps of: "transferring the integrated circuit from the integrated circuit singulation apparatus; receiving the integrated circuit at the testing apparatus while...in the first position; moving the testing apparatus to the second position; testing the integrated circuit thereby identifying defective and non-defective conditions thereof; moving the testing apparatus to the first position...allowing the tested integrated circuit to proceed to the holding station; receiving a second singulated integrated circuit into the testing apparatus...and separating the defective and non-defective integrated circuits." As previously explained, Tateno fails to disclose methods of "testing the integrated circuit thereby identifying defective and non-defective conditions thereof" and "separating the defective and non-defective integrated circuits." In addition, Tateno fails to disclose a step of "transferring the integrated

circuit from the integrated circuit singulation apparatus" to be received by the testing apparatus "while the testing apparatus is in the first position." Tateno's failure to disclose the steps of claim 16, as arranged in claim 16, bars an anticipation rejection of that claim under 35 U.S.C. § 102(b). Therefore, the rejection is improper and claim 16 is allowable.

(h) Claims 17 and 18

Claims 17 and 18 depend from claim 16, but do not stand or fall with claim 16. Claim 18 stands or falls with claim 17 which is independently patentable.

Claim 17 recites a method of testing an integrated circuit further including: "providing a testing apparatus with a non-defective and defective integrated circuit track; and...[preventing] defective integrated circuits from proceeding to the non-defective track, and allowing non-defective integrated circuits to proceed to the non-defective integrated circuit track." The absence of "a testing apparatus with a non-defective and defective integrated circuit track" from the Tateno disclosure or claims precludes a 35 U.S.C. § 102(b) rejection for anticipation because each and every element of the present invention is not disclosed as arranged in claim 17. Therefore, claim 17 is allowable. Likewise, claim 18, which depends from and stands or falls with claim 17, is allowable therewith.

(i) Claim 22

Claim 22 is an independently patentable method of testing an integrated circuit which includes the steps of testing an integrated circuit and separating defective integrated circuits from non-defective integrated circuits. Claim 22 further recites the step of "allowing the tested

integrated circuit to proceed to the holding station." This occurs after the testing step and prior to receiving a second integrated circuit for testing. As with the claims mentioned above, Tateno fails to anticipate the steps of "testing the integrated circuit thereby identifying defective and non-defective conditions thereof" and "separating the defective and non-defective integrated circuits." However, Tateno also fails to disclose a step "allowing the tested integrated circuit to proceed to the holding station" which is an additional limitation in claim 22. Because of Tateno's failure to anticipate claim 22, the rejection is invalid and claim 22 is allowable.

(j) Claims 23 and 24

Claims 23 and 24 depend from claim 22, but do not stand or fall with claim 22. Claim 24 stands or falls with claim 23 which is independently patentable.

Claim 23 recites a method of testing an integrated circuit further including: "providing a testing apparatus with a non-defective and defective integrated circuit track; and...[preventing] defective integrated circuits from proceeding to the non-defective track, and allowing non-defective integrated circuits to proceed to the non-defective integrated circuit track." The absence of "a testing apparatus with a non-defective and defective integrated circuit track" from the Tateno disclosure or claims precludes a 35 U.S.C. § 102(b) rejection for anticipation because each and every element of the present invention is not disclosed as arranged in claim 23. Therefore, claim 23 is allowable. Likewise, claim 24, which depends from and stands or falls with claim 23, is allowable therewith.

(k) Claims 25 and 26

Claim 26 depends from and stands or falls with claim 25, an independently patentable apparatus for testing singulated integrated circuits. The apparatus of claim 25 comprises: "a testing apparatus moveable between a first and second position...and a separating apparatus coupled to and movable between the first position and the second position." Tateno fails to disclose either a "testing apparatus" or a "separating apparatus" as in claim 25, thereby failing to anticipate claim 25 under 35 U.S.C. § 102(b). Because Tateno does not disclose the elements of claim 25, the anticipation rejection is invalid and claims 25 and 26 are allowable.

(l) Claim 27

Claim 27 is an independently patentable method of testing singulated integrated circuits comprising: "receiving an untested, singulated integrated circuit...while in the first position; moving the untested, singulated integrated circuit to the second position; testing the untested, singulated integrated circuit to determine first and second test conditions thereof; moving the tested, singulated integrated circuit back to the first position; allowing the tested, singulated integrated circuit to move to the holding station; receiving another untested, singulated integrated circuit...and separating the tested, singulated integrated circuits having the first test condition from integrated circuits having the second test condition." As previously detailed, Tateno fails to disclose either of the steps of testing or separating, tested integrated circuits. Tateno also fails to anticipate the testing of an integrated circuit "to determine first and second test conditions" which then determines how the tested integrated circuits are separated. In addition, Tateno fails to disclose the steps of "allowing the tested, singulated integrated circuit to move to the holding

station" and "receiving another untested, singulated integrated circuit...while in the first position." Tateno's failure to anticipate the steps detailed in claim 27 precludes an anticipation rejection based on 35 U.S.C. § 102(b). Claim 27 is allowable.

(m) Claim 28

Claim 28 depends from claim 27, however, claim 28 does not stand or fall with claim 27. Claim 28 is an independently patentable method of testing singulated integrated circuits because it further includes "releasing tested, singulated integrated circuits having the first test condition while the holding station is in the first position and releasing tested, singulated integrated circuits having the second test condition while the holding station is at the second position." A first and second position for the "holding station 50" of the Tateno apparatus is not disclosed, so the corresponding method steps cannot be met. In addition, Tateno fails to disclose a holding station which releases integrated circuits "having the first test condition while the holding station is in the first position" and those "having the second test condition" while the holding station is in a second position. Tateno's failure to anticipate the holding station of claim 28 precludes a proper rejection under 35 U.S.C. § 102(b), therefore, claim 28 is allowable.

(n) Claims 29 and 30

Claim 30 depends from, and stands or falls with claim 29, an independently patentable apparatus for testing singulated integrated circuits. The apparatus of claim 29 comprises: "a loading apparatus for supplying the integrated circuit leaving the integrated circuit singulation station to the integrated circuit testing apparatus; a testing apparatus moveable between a first and

second position receiving untested integrated circuits while in said first position and identifying first and second test conditions of an integrated circuit while in said second position; and a separating apparatus coupled to and movable between the first position and the second position." Tateno fails to disclose a "testing apparatus" capable of "identifying first and second test conditions." Tateno also fails to disclose a "separating apparatus" as in claim 29, thereby failing to anticipate claim 29 under 35 U.S.C. § 102(b). In addition, Tateno fails to anticipate a "loading apparatus for supplying" integrated circuits to the testing apparatus. Because Tateno does not disclose any of the elements of claim 29, the anticipation rejection is untenable and claims 29 and 30 are allowable.

(o) Claim 31

Claim 31 is an independently patentable method of testing an integrated circuit. Claim 31 recites a method of testing an integrated circuit comprising the steps of: "transferring the integrated circuit from the integrated circuit singulation apparatus; receiving an untested, singulated integrated circuit into the testing apparatus while in the first position; moving the untested, singulated integrated circuit to the second position; testing the untested, singulated integrated circuit to determine first and second test conditions thereof; moving the tested, singulated integrated circuit back to the first position; allowing the tested, singulated integrated circuit to move to the holding station; receiving another untested, singulated integrated circuit into the testing apparatus...and separating the tested, singulated integrated circuits having the first test condition from integrated circuits having the second test condition." Tateno fails to disclose methods of "testing the untested, singulated integrated circuit to determine first and second test

conditions thereof" and "separating the tested, singulated integrated circuits having the first test condition from integrated circuits having the second test condition." In addition, Tateno fails to disclose a step of "transferring the integrated circuit from the integrated circuit singulation apparatus" to be received by the testing apparatus "while the testing apparatus is in the first position," and the movement of an integrated circuit between a first position and second position for testing. Tateno's failure to disclose the steps of claim 31, as arranged in claim 31, bars an anticipation rejection of that claim under 35 U.S.C. § 102(b). Therefore, the rejection is improper and claim 31 is allowable.

(p) Claim 32

Claim 32 depends from claim 31, but does not stand or fall with claim 31. Claim 32 recites a method of testing singulated integrated circuits which further includes "releasing tested singulated integrated circuits having the first test condition while the holding station is in the first position and releasing tested, singulated integrated circuits having the second test condition while the holding station is at the second position." Tateno fails to disclose a "holding station 50" having a first and second position and thus cannot disclose the step of "releasing tested singulated integrated circuits having the first test condition while the holding station is in the first position and releasing tested, singulated integrated circuits having the second test condition while the holding station is at the second position." Thus, Tateno fails to anticipate claim 32. The rejection of claim 32 is improper and claim 32 is allowable.

(q) Conclusion

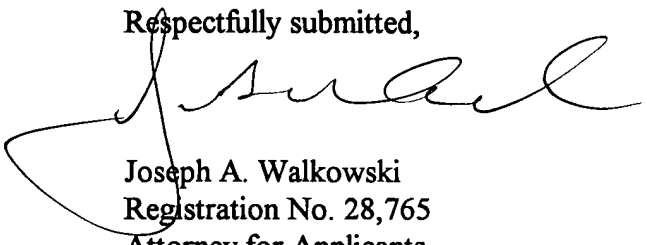
Tateno's failure to disclose both a testing apparatus and a separating apparatus and their operation as claimed in the present invention precludes the rejection of claims 7 through 32 under 35 U.S.C. § 102(b) for anticipation because each and every element of the present claims are not disclosed in Tateno. *See*, Verdegaal Brothers Inc. v. Union Oil Company of California, 2 USPQ2d 1051, 1053 (1987). Tateno's failure to disclose a "defective integrated circuit track...and a non-defective integrated circuit track," precludes the rejection of claims 7-12, 14-15, 17-18, 20-21, and 23-24 under 35 U.S.C. § 102(b) for anticipation because each and every element of the claimed invention is not disclosed in the prior art. *See*, Verdegaal Brothers Inc. v. Union Oil Company of California, 2 USPQ2d 1051, 1053 (1987). Additionally, Tateno's failure to claim a method of testing integrated circuits including such steps as "testing the integrated circuit to identify defective and non-defective conditions" or "separating the defective and non-defective integrated circuits" precludes the rejection of claims 13-24, 27-28, and 31-32 under 35 U.S.C. § 102(b) for anticipation because the each and every element of the claimed invention is not disclosed in the prior art. *See*, Verdegaal Brothers Inc. v. Union Oil Company of California, 2 USPQ2d 1051, 1053 (1987).

Therefore, claims 7-32 are patentable over Tateno, and the current Section 102(b) anticipation rejection should be reversed.

(9) APPENDIX

A copy of claims 7-32 is appended hereto as "Appendix A."

Respectfully submitted,



Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicants
TRASK, BRITT & ROSSA
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

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APPENDIX A

7. An integrated circuit testing apparatus for testing an integrated circuit leaving an integrated circuit singulation station, comprising:

a receiving apparatus positioned to receive untested integrated circuits from the integrated circuit singulation station;

a testing apparatus positioned to receive the untested integrated circuits from the receiving apparatus and test the integrated circuits to identify defective integrated circuits and non-defective integrated circuits, said testing apparatus including a holding station, a first position, and a second position, said testing apparatus while in said first position allowing tested integrated circuits to proceed to said holding station and allowing untested integrated circuits to be received from said receiving apparatus; and

a separating apparatus connected to the testing apparatus to separate defective integrated circuits from non-defective integrated circuits after testing thereof, said separating apparatus including a defective integrated circuit track for the defective integrated circuits and a non-defective integrated circuit track for the non-defective integrated circuits.

8. The apparatus of claim 7, wherein said testing apparatus while in said second position will electrically test the integrated circuit.

9. The apparatus of claim 8, further comprising:

the holding station while in the first position holding defective integrated circuits from proceeding

to the separating apparatus, and allow non-defective integrated circuits to proceed to the non-defective integrated circuit track of the separating apparatus; and

the holding station while in the second position releasing defective integrated circuits to the defective integrated circuit track of the separating apparatus.

10. An integrated circuit testing apparatus for testing an integrated circuit leaving an integrated circuit singulation station, comprising:

a loading apparatus for supplying the integrated circuit leaving the integrated circuit singulation station to the integrated circuit testing apparatus;

a receiving apparatus positioned to receive untested integrated circuits from the integrated circuit singulation station;

a testing apparatus positioned to receive the untested integrated circuits from the receiving apparatus and test the integrated circuits to identify defective integrated circuits and non-defective integrated circuits, said testing apparatus including a holding station, a first position, and a second position, said testing apparatus while in said first position allowing tested integrated circuits to proceed to said holding station and allowing untested integrated circuits to be received from said receiving apparatus; and

a separating apparatus connected to the testing apparatus to separate defective integrated circuits from non-defective integrated circuits after testing thereof, said separating apparatus including a defective integrated circuit track for the defective integrated circuits and a non-defective integrated circuit track for the non-defective integrated circuits.

11. The apparatus of claim 10, wherein said testing apparatus while in said second position will electrically test the integrated circuit.

12. The apparatus of claim 11, further comprising:

the holding station while in the first position holding defective integrated circuits from proceeding to the separating apparatus, and allow non-defective integrated circuits to proceed to the non-defective integrated circuit track of the separating apparatus; and

the holding station while in the second position releasing defective integrated circuits to the defective integrated circuit track of the separating apparatus.

13. A method of testing an integrated circuit in a testing apparatus having a test site, a holding station, a first position, and a second position, after the singulation of the integrated circuit in an integrated circuit singulation apparatus, said method comprising the steps of:

transferring the integrated circuit from the integrated circuit singulation apparatus;

receiving the integrated circuit at the testing apparatus while the testing apparatus is in the first position;

moving the testing apparatus to the second position;

testing the integrated circuit to identify defective and non-defective conditions of the integrated circuit;

moving the testing apparatus to the first position to allow the tested integrated circuit to proceed to the holding station while receiving a second singulated integrated circuit into the testing

apparatus; and

separating the defective and non-defective integrated circuits.

14. The method of claim 13, further including:

providing the testing apparatus with a non-defective and defective integrated circuit track; and

maintaining the holding station in the first position to prevent defective integrated circuits from proceeding to the non-defective track, and allowing non-defective integrated circuits to proceed to the non-defective integrated circuit track.

15. The method of claim 14 further including, moving the holding station to the second position and allowing the defective integrated circuit proceed to the defective integrated circuit track.

16. A method of testing an integrated circuit after the singulation thereof using a testing apparatus having a test site, a holding station, a first position, and a second position, said method comprising the steps of:

transferring the integrated circuit from the integrated circuit singulation apparatus;

receiving the integrated circuit at the testing apparatus while the testing apparatus is in the first position;

moving the testing apparatus to the second position;

testing the integrated circuit thereby identifying defective and non-defective conditions thereof;

moving the testing apparatus to the first position after testing of the integrated circuit;

allowing the tested integrated circuit to proceed to the holding station;

receiving a second singulated integrated circuit into the testing apparatus while in the first position; and

separating the defective and non-defective integrated circuits.

17. The method of claim 16, further including:

providing the testing apparatus with a non-defective and defective integrated circuit track; and

maintaining the holding station in the first position to prevent defective integrated circuits from proceeding to the non-defective track, and allowing non-defective integrated circuits to proceed to the non-defective integrated circuit track.

18. The method of claim 17 further including, moving the holding station to the second position and allowing the defective integrated circuit proceed to the defective integrated circuit track.

19. A method of testing an integrated circuit in a testing apparatus having a test site, a holding station, a first position, and a second position, after the singulation of the integrated circuit in an integrated circuit singulation apparatus, said method comprising the steps of:

receiving the integrated circuit at the testing apparatus while the testing apparatus is in the first position;

moving the testing apparatus to the second position;

testing the integrated circuit to identify defective and non-defective conditions of the integrated

circuit;

moving the testing apparatus to the first position to allow the tested integrated circuit to proceed to the holding station while receiving a second singulated integrated circuit into the testing apparatus; and

separating the defective and non-defective integrated circuits.

20. The method of claim 19, further including:

providing the testing apparatus with a non-defective and defective integrated circuit track; and

maintaining the holding station in the first position to prevent defective integrated circuits from proceeding to the non-defective track, and allowing non-defective integrated circuits to proceed to the non-defective integrated circuit track.

21. The method of claim 20 further including, moving the holding station to the second position and allowing the defective integrated circuit proceed to the defective integrated circuit track.

22. A method of testing an integrated circuit after the singulation thereof using a testing apparatus having a test site, a holding station, a first position, and a second position, said method comprising the steps of:

receiving the integrated circuit at the testing apparatus while the testing apparatus is in the first position;

moving the testing apparatus to the second position;

testing the integrated circuit thereby identifying defective and non-defective conditions thereof;

moving the testing apparatus to the first position after testing of the integrated circuit;

allowing the tested integrated circuit to proceed to the holding station;

receiving a second singulated integrated circuit into the testing apparatus while in the first position; and

separating the defective and non-defective integrated circuits.

23. The method of claim 22, further including:

providing the testing apparatus with a non-defective and defective integrated circuit track; and

maintaining the holding station in the first position to prevent defective integrated circuits from proceeding to the non-defective track, and allowing non-defective integrated circuits to proceed to the non-defective integrated circuit track.

24. The method of claim 23 further including, moving the holding station to the second position and allowing the defective integrated circuit proceed to the defective integrated circuit track.

25. An apparatus for testing singulated integrated circuits, comprising:

a testing apparatus movable between a first position and a second position receiving untested integrated circuits while in said first position and identifying first and second test conditions of an integrated circuit while in said second position; and

a separating apparatus coupled to and movable between the first position and the second position,

receiving tested integrated circuits from said testing apparatus while in said first position and releasing tested integrated circuits having the first test condition while at said first position and releasing tested integrated circuits having the second test condition while at said second position.

26. The apparatus of claim 25, wherein said testing apparatus and said separating apparatus include at least one integral member moveable between said first position and said second position.

27. A method of testing singulated integrated circuits in a testing apparatus having a first position, a second position, and a holding station, comprising:

receiving an untested, singulated integrated circuit into the testing apparatus while in the first position;

moving the untested, singulated integrated circuit to the second position;

testing the untested, singulated integrated circuit to determine first and second test conditions thereof;

moving the tested, singulated integrated circuit back to the first position;

allowing the tested, singulated integrated circuit to move to the holding station;

receiving another untested, singulated integrated circuit into the testing apparatus while in the first position; and

separating the tested, singulated integrated circuits having the first test condition from integrated circuits having the second test condition.

28. The method of claim 27, wherein said separating includes releasing tested, singulated integrated circuits having the first test condition while the holding station is in the first position and releasing tested, singulated integrated circuits having the second test condition while the holding station is at the second position.

29. An apparatus for testing singulated integrated circuits, comprising:

a loading apparatus for supplying the integrated circuit leaving the integrated circuit singulation station to the integrated circuit testing apparatus;

a testing apparatus movable between a first position and a second position receiving untested integrated circuits while in said first position and identifying first and second test conditions of an integrated circuit while in said second position; and

a separating apparatus coupled to and movable between the first position and the second position, receiving tested integrated circuits from said testing apparatus while in said first position and releasing tested integrated circuits having the first test condition while at said first position and releasing tested integrated circuits having the second test condition while at said second position.

30. The apparatus of claim 29, wherein said testing apparatus and said separating apparatus include at least one integral member moveable between said first position and said second position.

31. A method of testing singulated integrated circuits in a testing apparatus having a first position, a second position, and a holding station, comprising:

transferring the integrated circuit from the integrated circuit singulation apparatus;

receiving an untested, singulated integrated circuit into the testing apparatus while in the first position;

moving the untested, singulated integrated circuit to the second position;

testing the untested, singulated integrated circuit to determine first and second test conditions thereof;

moving the tested, singulated integrated circuit back to the first position;

allowing the tested, singulated integrated circuit to move to the holding station;

receiving another untested, singulated integrated circuit into the testing apparatus while in the first position; and

separating the tested, singulated integrated circuits having the first test condition from integrated circuits having the second test condition.

32. The method of claim 31, wherein said separating includes releasing tested, singulated integrated circuits having the first test condition while the holding station is in the first position and releasing tested, singulated integrated circuits having the second test condition while the holding station is at the second position.